GSFC MO&DSD TECHNOLOGY DEVELOPMENT PLAN

TITLE: **COMMUNICATIONS & DATA PROCESSING**	
NASA UPN: 315-90-17-03	WORK AREA MANAGER: Nicholas Speciale
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BRIEF TECHNICAL SUMMARY *(Objectives and Approach)*

The objective of this element is to implement future ultra-low cost CCSDS integrated ground systems. Effort begins with an implementation of a single-card 150 Mbps subsystem that integrates three current/9U Virtual Module Eurocard (VME) subsystems for frame synchronization, Reed-Solomon error correction, and CCSDS Services processing. The effort includes development and implementation of a system platform to support these new massively integrated CCSDS ground acquisition and processing subsystems. This effort also includes implementing other common ground data processing into the communication gateway system including a VLSI digital receiver. By digitally sampling signals immediately after they are down converted and providing demodulation, bit synchronization and Viterbi decoding, the communication gateway system will allow almost direct hook-up to antenna elements. Future efforts include the investigation of massive integration approaches for forward link and data simulation.

APPROVALS		
WORK AREA MANAGER:	DIVISION MANAGER:	GSFC PROGRAM MANAGER:

JUSTIFICATION AND BENEFITS

The present generation of VLSI data systems is gaining wide acceptance by the NASA community. A large part of this success can be attributed to the significant cost and complexity reduction that these systems offer over alternative implementations, as well as their capability to handle time division multiplexing of data streams using Nascom and CCSDS protocols. However, the fundamental technologies that have enabled such reductions are over five years old. In this time period, VLSI technology has progressed very rapidly. Commercially available chip densities are ten to thirty times greater today than when the first chips for present generation VLSI data systems were developed. Using today's technologies, it is possible to implement a new generation of VLSI data systems that offer a sizable advantage over present systems by further lowering cost and complexity while increasing functionality and performance.

This element will make use of these massive integration levels available from commercial VLSI foundries to develop a lower cost, less complex solution for handling forward and return CCSDS telemetry streams. The final product of this effort, the communications gateway system prototype, will be very compact by today's standards and will plug into a standard 120 volt wall outlet. The system will perform synchronization, error correction, and CCSDS service processing before transferring data through a standard commercial network interface. The system will seamlessly connect to an operator who will be supplied with a standard graphical interface that features elements for highly automated configuration and control of the system.

APPROACH AND PLAN

Task 1 - Communications Gateway

Communications gateway systems are targeted for use in a wide range of operational environments so that they can be used as "building blocks" in large multistring institutional facilities or as standalone processing systems in direct broadcast and spacecraft integration applications. The ultra-low cost of this system is not only expected to reduce specific project costs in development, maintenance, and operation of ground processing environments, but also to promote even greater overall savings through the wide-scale standardization of data system elements across projects.

Subtask 1 - CCSDS Processor PCI Board Development

This task focuses on integrating the Parallel Integrated Frame Synchronizer chip, the Reed-Solomon Error Correction chip, and the Service Processor chip onto a single board that plugs into

any personal computer using the PCI bus standard. Part of this task is the development of "plug-and-play" software to allow setup, control and integration of this card into systems. The goal of

this task is to demonstrate high performance (over 300 Mbps) baseband CCSDS return link processing.

Subtask 2- Service Processor ASIC Chip Development

The goal of this task is to develop a high integration VLSI chip that performs CCSDS service processing. The Service Processor Application Specific Integrated Circuit (ASIC) will be highly programmable and will handle all standard CCSDS AOS (Advanced Orbiting Spacecraft) return link services including packet extraction and re-assembly. It will operate at nominal packet rates over 1 million packets per second and data rates to 300 Mbps.

Task 2 - High Rate CMOS Digital Receiver (HRCDR)

Current and future requirements for Low Earth Orbit (LEO) satellites are driving needs for ultra-low cost ground station acquisition and processing elements. Demand for low-cost ground stations is illustrated in LEO-D and LEO-T ground station development activities. While these efforts represent a potential cost savings over currently deployed systems, even greater savings can be achieved through further integration of ground station processing elements. This effort proposes the use of 'system-in-a-chip' VLSI technology to dramatically reduce the cost and size of ground station signal processing elements.

High integration VLSI technology has been used to reduce ground system protocol processing subsystem replication costs by as much as 75%. Continued application of highly integrated 'system-in-a-chip' VLSI technology is expected to yield an additional cost saving of 50 - 80%. This effort proposes the use of similar techniques to reduce the cost and size of ground station receivers. Current ground based receivers typically use discrete circuitry for demodulation and symbol or bit synchronization that span multiple subsystem elements. This effort will use novel parallel digital signal processing algorithms, pipelined multi-processing, and low-cost commercial digital CMOS ASIC technology to shrink several current subsystems into a single component while providing higher performance.

The objective of the High Rate CMOS Digital Receiver (HRCDR) is to develop a digital receiver prototype using highly integrated processing elements implemented on an ASIC in a parallel fashion. This array will implement a parallel digital filter bank that performs BPSK or QPSK demodulation, carrier tracking and symbol (or bit) synchronization at a down-converted intermediate frequency (IF). The key feature of this implementation is that the processing rate through any single filter bank is less than the aggregate output symbol or bit rate. As such, it allows multiple low rate processing elements (less than 20 Mbps each) to be used in parallel to process very high data rate signals (150 Mbps and beyond).

The approach for the development of the HRCDR involves three steps. The first step is to build upon the prototype architecture and algorithms developed jointly by GSFC and JPL. The second step is to translate this architecture into a 'system-in-a-chip' VLSI component. The third step is to integrate the ASIC onto a prototype board for testing.

Subtask 1 - High Rate CMOS Digital Receiver Architecture and Algorithm Development

This task will focus on continuing the development of the prototype parallel, digital architecture and associated algorithms for performing demodulation, carrier tracking and bit synchronization. The architecture is being prototyped using Field Programmable Gate Arrays (FPGAs). This architecture will demonstrate key features that will provide significantly lower cost / higher performance than receivers currently available today or in the near future:

a. High degree of parallelism: The architecture provides the required functions utilizing decimated samples of the input signal and then reconstruct the full output signal by combining multiple streams.

b. Efficient hardware implementation: The architecture lends itself to translation into CMOS ASIC technology. A more compact and less transistor intensive algorithm will result in a lower cost / higher performance chip.

c. Flexibility: The architecture accommodates various signal formats and modulation schemes to allow its application to multiple existing and future space missions.

Subtask 2 - HRCDR ASIC Chip Development

This task focuses on developing a HRCDR chip that will accept a decimated digital sample of the input data stream. The input samples are decimated by 16 which allows the chip to process the samples at 1/4 of the data rate. By decreasing the clock rate of the chip by 1/4 of the data rate, up to 300 Msamples/sec per channel can be achieved. Using both the I & Q channels of QPSK modulated data, the total processing rate can go as high as 600 Msamples/sec. This chip will be implemented using commercial 0.3 micron CMOS technology.

Subtask 3 - HRCDR PCI Board Development

This task focuses on integrating two HRCDR chips onto a single board that plugs into in any personal computer using the PCI bus standard. Initial data rates for this board are expected to exceed 30 Mbps. The input of the board will feature a commercial A/D converter running a minimum of 140 MHz. The samples from this device will be distributed to two HRCDR chips that perform the receiver and bit synchronizer functions. The data will be Viterbi decoded and the resulting bits will be made available to the PCI (Personal Computer Interface) bus or to a connec-

tor on the back panel. Part of this task is the development of "plug-and-play" software to allow setup, control and integration of this card into systems. This card will be designed to connect directly inside the Communications Gateway System (being developed under a separate effort). The combination of these two efforts will demonstrate a single compact system that hooks up to antenna system elements, processes incoming modulated signals, and provides extracted packet data to users over a commercial network interface. The estimated replication cost of the entire system is less than $40K.

DELIVERABLES

ITEM	DATE
Task 1 - Communications Gateway	
Sub-Task 1:	
a. Present Critical Design Review for CCSDS processor card	10/96
b. Complete design and fabrication of CCSDS processor card.	01/97
c. Integrate and test Communications Gateway Platform	04/97
Sub-Task 2:	
d. Complete design, fabrication and test of chip	12/96
Task 2 - High Rate CMOS Digital Receiver	
Sub-Task 1:	
a. Prototype FPGA Board of Architecture	04/97
Sub-Task 2:	
b. HRCDR ASIC Chip Development	10/97
Sub-Task 3:	
c. HRCDR PCI Board Development	01/98
d. Prototype Demonstration	01/98

RESOURCE REQUIREMENTS

Task Name	**NASA UPN**	**FY97** *($K)*	**FY98** *($K)*	**FY99** *($K)*	**FY00** *($K)*	**FY01** *($K)*	**FY02** *($K)*
Communications & Data Processing	(315-90-17-03)	325	435	410	450	450	450

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UPN: 315-90-17-03: COMMUNICATIONS & DATA PROCESSING

SCHEDULE

COMMUNICATIONS & DATA PROCESSING	FY97				FY98		FY99	FY00	FY01	FY02
	Q1	Q2	Q3	Q4	Q1/2	Q3/4				
Communications Gateway										
a. CCSDS Processor Card CDR										
b. Design & Fab. of CCSDS Proc. Card										
c. Integ. & Test Comm. Gateway Platform										
d. Complete design, fab. & test of chip										
High Rate Parallel Digital Receiver										
a. Prototype FPGA Board Architecture										
b. HRCDR ASIC Development										
c. HRCDR PCI Board Development										
d. Prototype Demonstration										
Resources by FY ($K):	325				435		410	450	450	450